REMARKS

Applicant has reviewed and considered the Office Action mailed on March 26, 2003, and the references cited therewith.

No claims are amended, no claims are canceled, and no claims are added; as a result, claims 1-25 remain pending in this application.

§103 Rejection of the Claims

Claims 1-25 were rejected under 35 USC § 103(a) as being unpatentable over Robinson et al. (U.S. Patent No. 5,524,244) in view of Ho (U.S. Patent No. 6,421,814). Applicant respectively traverses these rejections.

Claim 1, in part, recites "a global file of global geometric variables relating to a physical layout of element blocks of the hierarchical semiconductor structure."

Applicant can not find in Robinson et al. (hereafter Robinson) a teaching or suggestion of geometric variables related to the physical layout of a hierarchical semiconductor structure, as recited in claim 1. The Examiner apparently agrees stating "Robinson does not expressly disclose geometric variables related to physical layout in hierarchical manner as claimed." Further, Applicant can not find a teaching or suggestion in Robinson regarding a "hierarchical semiconductor structure." Robinson's hierarchical discussions deal with a signal processing design. *See Robinson, column 79, line52-54.* Further, Robinson uses hierarchical blocks with respect to an order of activation, "firing order," and partitioning. *See, column 59, lines 36-56.*

Applicant can not find in Ho a teaching or suggestion of geometric variables related to the physical layout of a hierarchical semiconductor structure, as recited in claim 1. Though Ho may discuss device parameters, which may include geometric variables in a semiconductor structure, Applicant can not find in Ho a teaching or suggestion relating such device parameters in a local file to device parameters in global file in a manner as recited in claim 1. Further, Applicant can not find a teaching or suggestion in Ho regarding a hierarchical semiconductor structure, or geometric variables related to a physical layout in a hierarchical semiconductor structures. In discussions with respect to Figures 19-21, Ho refers to hierarchical blocks in an integrated circuit. *See, column 11, lines 16-28.* Reviewing this discussion and associated figures,

it appears that the hierarchical process of Ho deals with a hierarchical block structure of the circuitry of an integrated circuit which is distinctly different than a hierarchical semiconductor structure. Though Ho may use geometric variables in extracting parameters relative to a hierarchical circuit layout, Ho appears not use these geometric variables in a physical layout in a hierarchical semiconductor structure. Thus, Ho does not cure the above-mentioned deficiencies of Robinson.

Since Robinson deals with hierarchical blocks in a signal processing design, and Ho briefly discusses a hierarchical block structure of circuitry of an integrated circuit, the combination of Robinson and Ho does not teach or suggest geometric variables relating to a physical layout in a hierarchical semiconductor structure. Thus, Applicant submits that the combination of Robinson and Ho does not teach or suggest all the elements of claim 1, and therefore, claim 1 is patentable over Robinson in view of Ho.

Further, the combination of Robinson with Ho is not proper since there is no suggestion to combine the cited references, because a suggestion to combine must come from the prior art and not from Applicant's specification or impermissible hindsight. The Office Action states that

> "[t]his would motivate practitioner in the art at the time of the invention was made to use Ho teaching of geometrical layout file and geometrical shape variables in hierarchical relationships for physical design of the integrated circuit as disclosed in Robinson to improve physical design and circuit compile process to produce a final circuit to meet specification requirement because Robinson discloses method and system for passing design parameters through file hierarchical relations. Such design parameters could include physical parameters cell shapes, sizes, etc, (Ho)."

Applicant can not find a teaching or suggestion for a physical design of an integrated circuit disclosed in Robinson as proposed in this quote (Robinson appears to deal with "a system which provides the realization of a high level circuit in a silicon chip." *See, column 83, lines 47- 49*). Further, Applicant can not find where Robinson discloses a method and system for passing geometric variables for the physical layout of a hierarchical semiconductor structure. Combining Ho's device parameters with Robinson's signal processing approach would appear to result in extraneous data for Robinson's system and method, since Robinson appears not to deal with an integrated circuit at the geometric and physical level. Applicant can not find in the cited references or in the Office Action any reasons that would indicate that the Ho device parameters

could be utilized in Robinson' method and system, as proposed by the Office Action. The Office Action has provided no objective reference or a specific reason to support the proposition that Robinson can pass design parameters where "[s]uch design parameters could include physical parameters cell shapes, sizes, etc, (Ho)." The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, not in applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991); MPEP § 2143. Since no reasonable expectation of success has been provided for the combination of Robinson with Ho as proposed in the Office Action, Applicant submits that such combination is not proper.

For the reasons stated above, Applicant submits that claim 1 is patentable over Robinson in view of Ho. Claims 9, 15, and 22 recite similar elements as claim 1, and are patentable over Robinson in view of Ho for the reasons stated above in addition to the elements of these claims.

Claims 2-8, 10-14, 16-21 and 23-25 depend, directly or indirectly, on claims 1, 9, 15 and 22, respectively, and are patentable over Robinson in view of Ho for the reasons stated above in addition to the elements in these claims.

Applicant respectfully requests withdrawal of these rejections of claims 1-25, and reconsideration and allowance of these claims.

Assertion of Pertinence

Applicant has not responded to the assertion of pertinence stated for the patents cited but not relied upon by the Office Action since these patents are not relied upon as part of the rejections in this Office Action. Applicant is expressly not admitting to any assertion of their pertinence and reserves the right to address the assertion should it form a part of some future rejection.

CONCLUSION

Applicant respectfully submits that the claims are in condition for allowance and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's attorney at (612) 371-2157 to facilitate prosecution of this application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

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Date 27 MAY 2003

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CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Mail Stop AF, Commissioner of Patents, P.O.Box 1450, Alexandria, VA 22313-1450, on this 27 day of May, 2003

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